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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/826,661	04/05/2001	Yongjun Hu	303.098US4	4539

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EXAMINER	
NGUYEN, JOSEPH H	
ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 04/24/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/826,661	HU, YONGJUN	
	Examiner	Art Unit	
	Joseph Nguyen	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *31-37 and 39-70* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *31-37 and 39-70* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 31-34, 36-37, 39-47, 55-58, 59-70 are rejected under 35 U.S.C. 102(e) as being anticipated by Miyamoto.

Regarding claims 31, Miyamoto discloses on figure 3 a contact hole for a semiconductor device comprising "a bottom surface of a first material [1]; at least one vertical sidewall of a second insulating material [2]; a generally planar layer of a third conductive material [6] covering only the bottom surface, the third material including at least two different constituent elements".

Regarding claim 32, Miyamoto discloses the third material 6 is an alloy or a composite (col. 8, line 49).

Regarding claim 33, Miyamoto discloses the third material 6 contains a refractory metal (col. 8, line 49).

Regarding claim 34, Miyamoto discloses third material 6 is a silicide (col. 8, line 49).

Regarding claim 36, Miyamoto discloses the stoichiometry of the third layer 6 is uniform (col. 5, lines 3-4).

Regarding claim 37, Miyamoto discloses on figure 3 the first material 1 is silicon.

Regarding claim 39, Miyamoto discloses on figure 3 a contact hole for a semiconductor device comprising a bottom surface of a first material 1; at least one vertical sidewall of a second insulating material 2 and having a high aspect ratio; a generally planar layer of a third material 6 covering only the bottom surface, the third material including at least two different constituent elements.

Regarding claim 40, Miyamoto discloses on figure 3 a height of the sidewall is at least four times a width of the bottom surface (col. 9, lines 4-8).

Regarding claim 41, Miyamoto discloses a width of the bottom surface is equal or less than about 0.5 microns (col. 9, line 6).

Regarding claim 42, Miyamoto discloses on figure 3 the third material 6 is substantially confined to the bottom surface of the hole.

Regarding claim 43, Miyamoto discloses on figure 3 a contact hole for a semiconductor device comprising "a bottom surface of a first material [1]; at least one vertical sidewall of a second material [2]; a generally planar layer of a third material [6] covering only the bottom surface with a thickness variation of less than 50% [col.5, lines 3-4], the third material including at least two different constituent elements".

Regarding claims 44 -45, Miyamoto discloses the thickness variation of the layer is less than about 20% and 10% (col. 5, lines 3-4).

Regarding claim 46, Miyamoto discloses on figure 3 the planar layer 6 contacts the sidewalls.

Regarding claim 47, Miyamoto discloses on figure 3 the planar layer 6 does not extend to a substantial distance up the sidewall from the bottom.

Regarding claim 55, Miyamoto discloses a contact hole for a semiconductor device comprising a bottom surface of a first material 1; at least one sidewall of an insulating material 2; a generally planar layer of a third material 6 covering only the bottom surface, the third material including at least two different constituent elements, none of the third material 6 being present in the sidewall.

Regarding claim 56, Miyamoto discloses the insulator 2 is an oxide (col. 8, line 37).

Regarding claim 57, Miyamoto discloses on figure 3 the layer of the third does not extend substantially up the sidewall from the bottom.

Regarding claim 58, Miyamoto discloses the third material 6 is a silicide.

Regarding claim 59, Miyamoto discloses on figure 3 an integrated circuit comprising a substrate 1 of a first material; an insulator 2 of a second material overlying the substrate; a contact hole through the insulator to the substrate, the contact hole having at least one sidewall of the second material and a generally planar conductive layer 36 located only in a region contacting the substrate, the layer including at least two different constituent elements.

Regarding claim 60, Miyamoto discloses on figure 3 the substrate is silicon.

Regarding claim 61, Miyamoto discloses on figure 3 the second material is an oxide.

Regarding claim 62, Miyamoto discloses on figure 3 the planar layer 6 contacts the sidewall.

Regarding claim 63, Miyamoto discloses on figure 3 the layer 6 is planar within a thickness variation less than 50%.

Regarding claim 64, Miyamoto discloses on figure 3 the layer 6 is planar within a thickness variation of about 20%.

Regarding claim 65, Miyamoto discloses on figure 3 an integrated circuit comprising a substrate 1 of a first material; an insulator 2 of a second material overlying the substrate; a contact hole through the insulator to the substrate 1, the contact hole having at least one sidewall of the second material and a separate generally planar layer 6 of a silicide contacting only the substrate.

Regarding claim 66, Miyamoto discloses on figure 3 the silicide includes a refractory metal.

Regarding claim 67, Miyamoto discloses on figure 3 the refractory metal is titanium.

Regarding claim 68, Miyamoto discloses on figure 3 the silicide has a uniform stochiometry.

Regarding claim 69, Miyamoto discloses on figure 3 the silicide has at least two different stoichiometries.

Regarding claim 70, Miyamoto discloses on figure 3 the insulator has the top surface free of the silicide.

Claims 31-35, 37, 42, 48, 50- 54, 56- 70 are rejected under 35 U.S.C. 102(e) as being anticipated by Chen.

Regarding claims 31, Chen discloses on figure 3B a contact hole for a semiconductor device comprising "a bottom surface of a first material [31]; at least one vertical sidewall of a second insulating material [33]; a generally planar layer of a third material [36] covering only the bottom surface, the third material including at least two different constituent elements".

Regarding claim 32, Chen discloses the third material 36 is an alloy or a composite (col. 3, line 44).

Regarding claim 33, Chen discloses the third material 36 contains a refractory metal (col. 3, line 44).

Regarding claim 34, Chen discloses third material 36 is a silicide (col. 3, line 44).

Regarding claim 35, Chen discloses the third material 36 is rich in titanium (col. 3, line 44).

Regarding claim 37, Chen discloses on figure 3B the first material 31 is silicon.

Regarding claim 39, Chen discloses on figure 3B a contact hole for a semiconductor device comprising a bottom surface of a first material 31; at least one vertical sidewall of a second insulating material 33 and having a high aspect ratio; a

generally planar layer of a third material 36 covering only the bottom surface, the third material including at least two different constituent elements.

Regarding claim 42, Chen discloses on figure 3B the third material 36 is substantially confined to the bottom surface of the hole.

Regarding claim 48, Chen discloses on figure 3B a contact hole for a semiconductor device comprising "a bottom surface of a first material [31]; at least one vertical sidewall of a second material [33]; a generally planar layer of a third material covering only the bottom surface, the third material [36] having a graded stoichiometry (col. 4, lines 7-12) between two different elements".

Regarding claim 50, Chen discloses the first material 31 is silicon.

Regarding claim 51, Chen discloses the second material 33 is an insulator.

Regarding claim 52, Chen discloses the planar layer 36 contacts the sidewalls.

Regarding claim 53, Chen discloses the third material 36 is substantially confined to the bottom of the hole.

Regarding claim 54, Chen discloses the third material 36 is a silicide.

Regarding claim 55, Chen discloses on figure 3B a contact hole for a semiconductor device comprising a bottom surface of a first material 31; at least one sidewall of an insulating material 33; a generally planar layer of a third material 36 covering only the bottom surface, the third material having at least two different constituent element, none of the third material 36 being present in the sidewall.

Regarding claim 56, Chen discloses the insulator 33 is a glass.

Regarding claim 57, Chen discloses on figure 3B the layer of the third does not extend substantially up the sidewall from the bottom.

Regarding claim 58, Chen discloses the third material 6 is a silicide.

Regarding claim 59, Chen discloses on figure 3B an integrated circuit comprising a substrate 31 of a first material; an insulator 33 of a second material overlying the substrate; a contact hole through the insulator to the substrate, the contact hole having at least one sidewall of the second material and a generally planar conductive layer 36 located only in a region contacting the substrate, the layer including at least two different constituent elements.

Regarding claim 60, Chen discloses on figure 3B the substrate is silicon.

Regarding claim 61, Chen discloses on figure 3B the second material is an oxide.

Regarding claim 62, Chen discloses on figure 3B the planar layer 36 contacts the sidewall.

Regarding claim 63, Chen discloses on figure 3B the layer 36 is planar within a thickness variation less than 50%.

Regarding claim 64, Chen discloses on figure 3 the layer 36 is planar within a thickness variation of about 20%.

Regarding claim 65, Chen discloses on figure 3B an integrated circuit comprising a substrate 31 of a first material; an insulator 33 of a second material overlying the substrate; a contact hole through the insulator to the substrate 31, the contact hole having at least one sidewall of the second material and a separate generally planar layer 6 of a silicide contacting only the substrate.

Regarding claim 66, Chen discloses on figure 3B the silicide includes a refractory metal.

Regarding claim 67, Chen discloses on figure 3B the refractory metal is titanium.

Regarding claim 68, Chen discloses on figure 3B the silicide has a uniform stochiometry.

Regarding claim 69, Chen discloses on figure 3B the silicide has at least two different stoichiometries.

Regarding claim 70, Chen discloses on figure 3B the insulator has the top surface free of the silicide.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 49 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen as applied to claim 48 above, and further in view of Miyamoto.

Regarding claim 49, Chen discloses substantially all the structure set forth in the claimed invention except the hole having a high aspect ratio. However, Miyamoto discloses on figure 3 the hole having a high aspect ratio (col. 9, lines 3-8). In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Miyamoto by having the hole having a high aspect

ratio for the purpose of providing a good coverage over a surface of the silicon substrate.

Response to Arguments

Applicant's arguments filed on 2/20/2002 have been fully considered but they are not persuasive.

With respect to claim 31, applicant argues that neither Miyamoto nor Chen discloses the conductive layer covers *only* the bottom surface. However, Miyamoto clearly discloses on figure 3 the conductive layer 6 covers only the bottom surface. Note that the layer 5 (titanium) in figure 3 of Miyamoto is not the same material as the layer 6 (titanium silicide), and therefore the layer 6 of the same material covers only the bottom surface and not on the sidewall of the insulating layer 2. In the same way, Chen clearly discloses on figure 3B the conductive layer 36 covers only the bottom surface.

With respect to claim 49, since Chen still discloses the structure of claim 48, the combination of Chen and Miyamoto clearly discloses the structure of claim 49.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Nguyen whose telephone number is (703) 308-1269. The examiner can normally be reached on Monday-Friday, 7:30 am- 4:30 pm

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 308-7382 for regular communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JN
April 22, 2002

EDDIE LEE
SUPERVISORY PATENT EXAMINER
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